Model Analysis

- Once an entity is described in VHDL, it can be validated using an analyzer and a simulator that are part of a VHDL system.
- The analyzer takes a file that contains one or more design units and compiles them into an intermediate form.
- During compilation, the analyzer validates the syntax and performs static semantic checks.

Model Analysis cont..

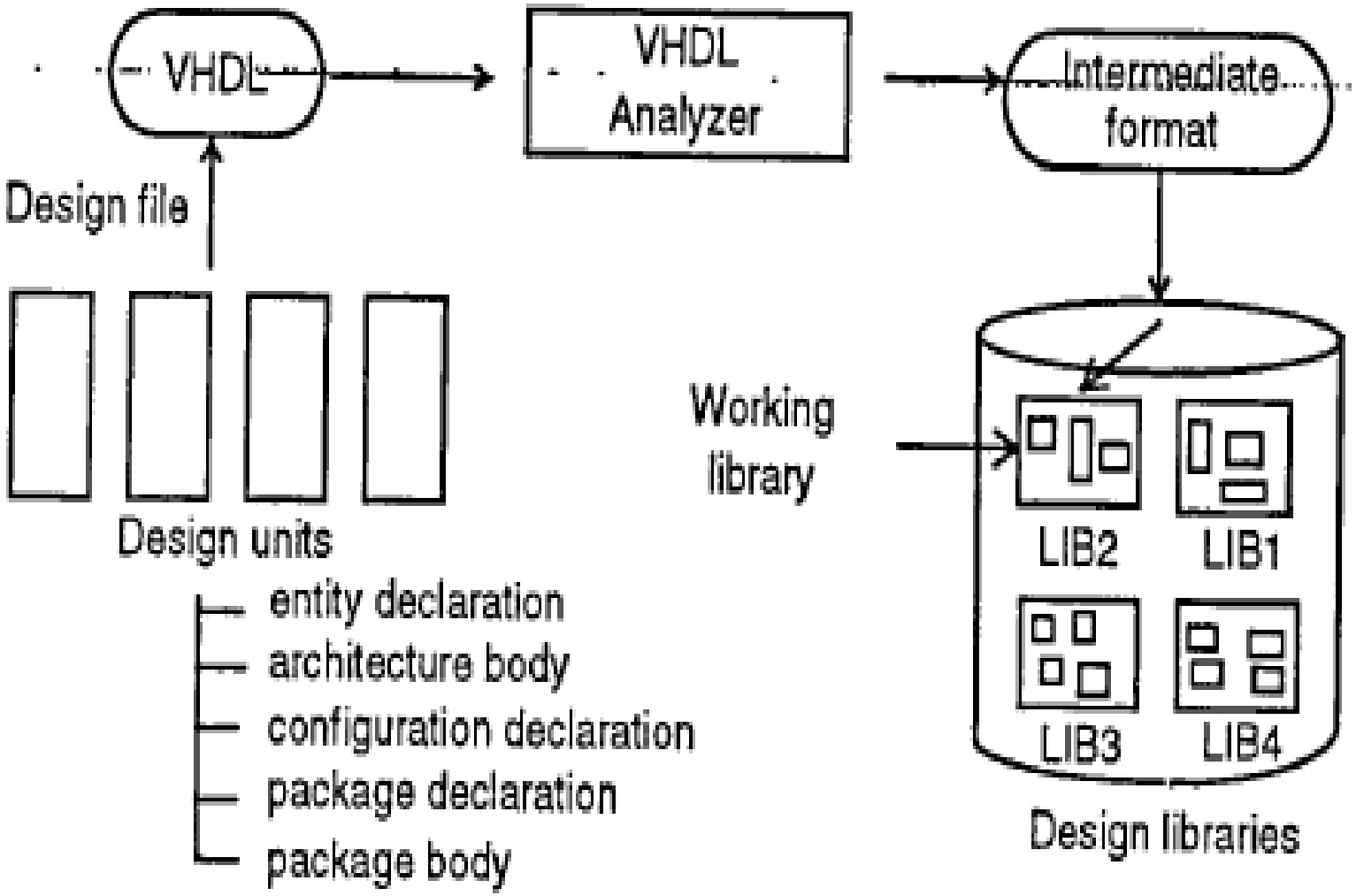

Figure 2.8 The compilation process.

Model Analysis cont..

- The generated intermediate form is stored in a specific design library, that has been designated as the working library.
- A design library is a location in the host environment (the environment that supports the VHDL system) where compiled descriptions are stored.

Simulation

- Once the model description is successfully compiled into one or more design libraries, the next step in the validation process is simulation.

- A simulation can be performed on either one of the following:
- an entity declaration and an architecture body pair,
- **a configuration.**

Simulation cont..

Actual simulation consists two major steps:

1. *Elaboration phase*
2. *Initialization phase*

Simulation cont..

1. *Elaboration phase: In this phase, the hierarchy of the entity is expanded and linked, components are bound to entities in a library .Also storage is allocated for all data objects (signals, variables, and constants) declared in the design units. Initial values are also assigned to these objects.*

Simulation cont..

2. *Initialization phase: The effective values for all explicitly declared signals are computed, are assigned values, processes are executed once until they suspend, and simulation time is reset to 0 ns.*